PI49FCT807T

Fast CMOS Clock Driver

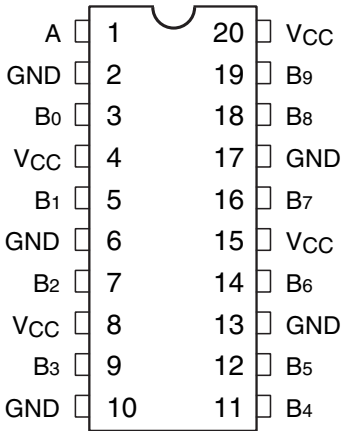
Features

- Guaranteed low skew: 0.25ns
- Low input capacitance
- Minimum duty cycle distortion
- 1:10 fanout
- High speed: 3.5ns propagation delay
- TTL input and CMOS output compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Industrial Operation at -40ºC to +85ºC
- Packaging (Pb-free & Green available):
  - 20-pin 150-mil wide QSOP (Q)
  - 20-pin 209-mil wde SSOP (H)

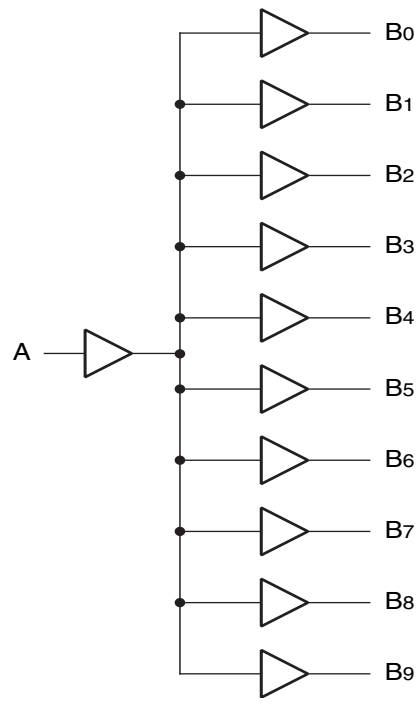
Description

Pericom Semiconductor's PI49FCT807T clock driver feature one input and ten outputs. The large fanout from a single input line reduces loading on input clock. TTL level outputs reduce noise levels on the part. Typical applications are clock and signal distribution.

Pin Configuration



Block Diagram



Pin Description

Pin Name	Description
A	Input
B0 - B9	Outputs
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V_{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 40°C to +85°C, V_{CC} = 5.0V ±5%)

Parameters	Description	Test Conditions[1]		Min	Typ[2]	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC}=Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0mA	2.4	3.3		V
V_{OL}	Output LOW Current	V_{CC}=Min., V_{IN} = V_{IH} or V_{IL}	I_{OL}= 48.0mA		0.2	0.5	V
			I_{OL} = 12mA			0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = 2.7V			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = 0.5V			-1	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} =V_{CC} (Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		-60	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND			-120		mA
I_{OFF}	Power Down Disable	V_{CC}= GND, V_{OUT} = 4.5V				100	µA
V_H	Input Hysteresis				150		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6.0	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max	V_{IN} = GND or V_{CC}		3	30	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open 50% Duty Cycle, Per Output Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.4	0.6	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 50 MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		20	30[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		20.7	33[5]	

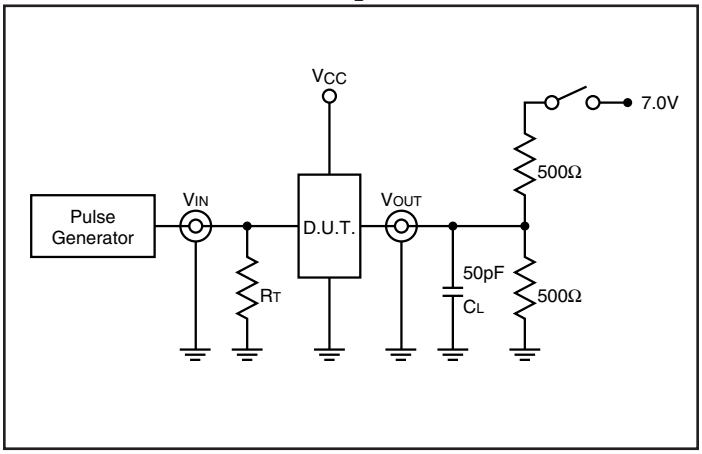
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	807/2807T		807AT		807BT		807CT		Units
			Com.		Com.		Com.		Com.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B_N	C_L = 50pF R_L = 500Ω	1.5	4.5	1.5	4.0	1.5	3.8	1.5	3.5	ns
$t_{SK(o)}$	Skew between two outputs of same package[3]			0.5		0.5		0.35		0.25	ns
$t_{SK(p)}$	Skew between opposite transitions of same output (|tPHL — tPLH|)[3]			0.5		0.5		0.35		0.35	ns
$t_{SK(t)}$	Skew between outputs of different package at same power supply, temperature and speed grade[3]			1.0		1.0		0.75		0.75	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Tests Circuits For All Outputs(1)



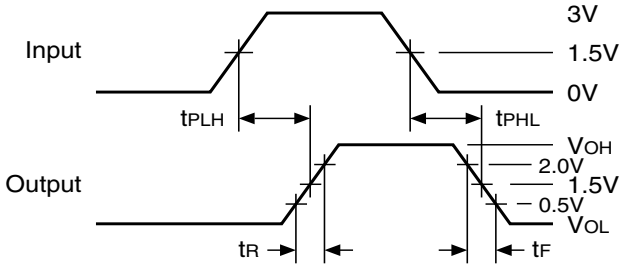
Switch Position

Test	Switch
Open Drain Disable LOW Enable LOW	Closed
All Other Inputs	Open

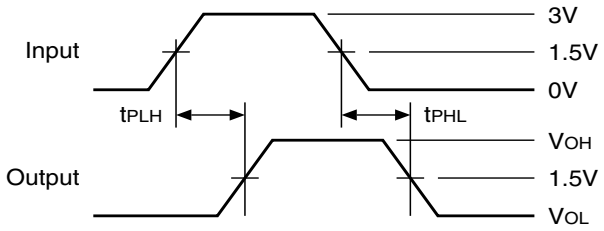
Definitions:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to ZOUT of the Pulse Generator.

Switching Waveforms

Propagation Delay

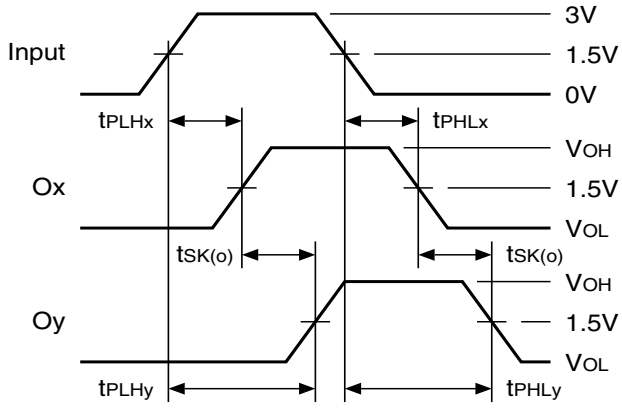


Pulse Skew – $t_{SK(p)}$



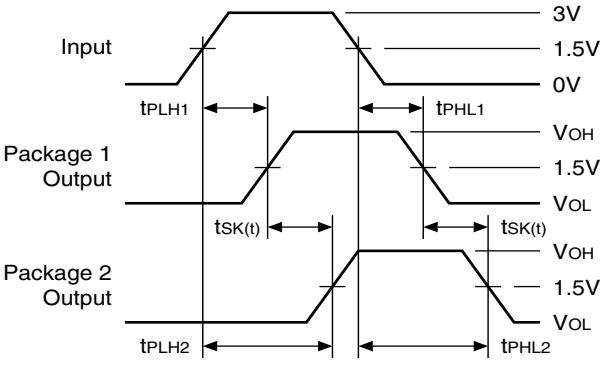
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Output Skew – $t_{SK(o)}$



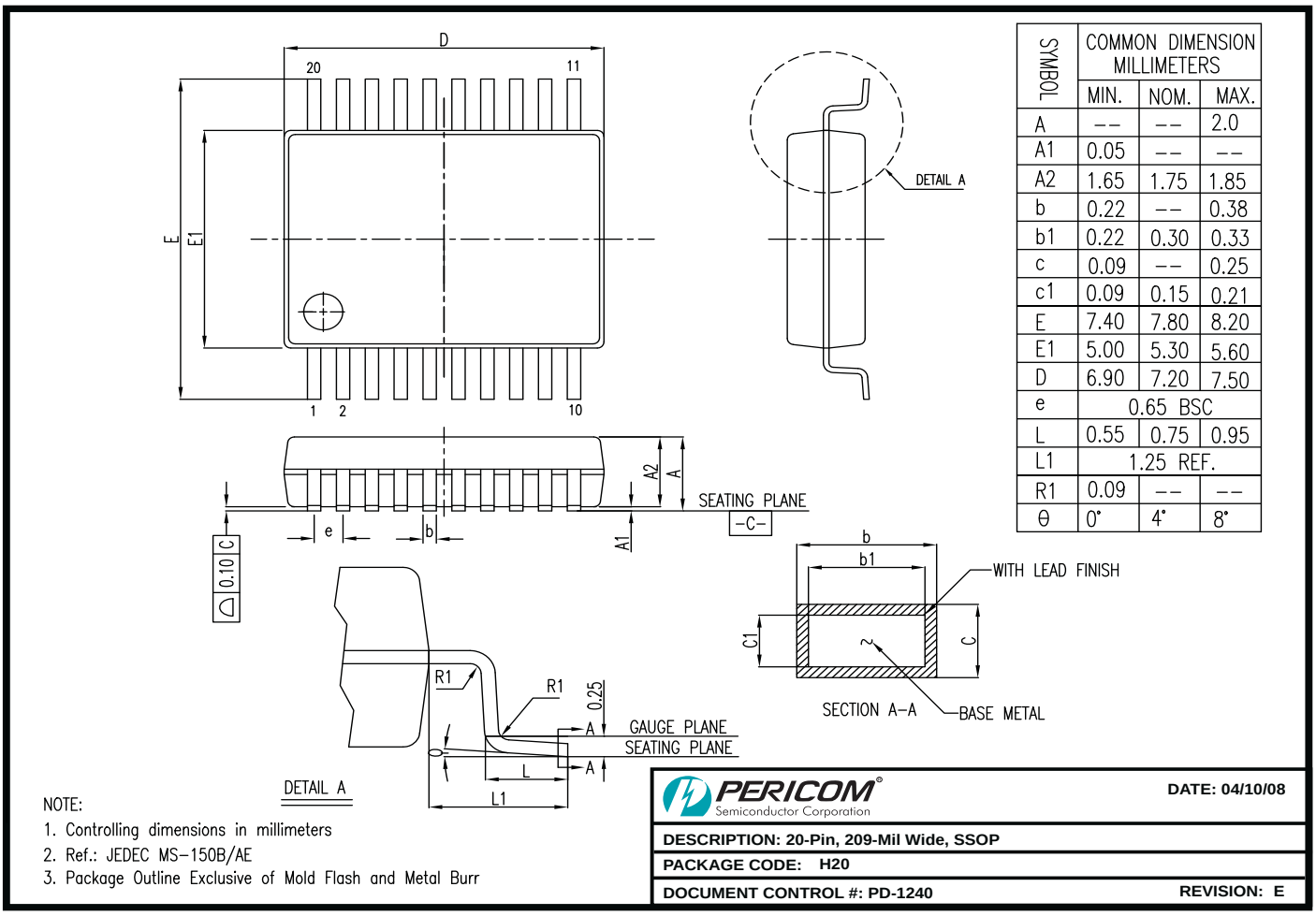
$t_{SK(o)} = |t_{PLHy} - t_{PLHx}|$ or $|t_{PHLy} - t_{PHLx}|$

Package Skew – $t_{SK(t)}$



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Packaging Mechanical: 20-Pin 209-Mil SSOP (H)



SYMBOL	COMMON DIMENSION MILLIMETERS		
	MIN.	NOM.	MAX.
A	--	--	2.0
A1	0.05	--	--
A2	1.65	1.75	1.85
b	0.22	--	0.38
b1	0.22	0.30	0.33
c	0.09	--	0.25
c1	0.09	0.15	0.21
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
D	6.90	7.20	7.50
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25 REF.		
R1	0.09	--	--
θ	0°	4°	8°

NOTE:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-150B/AE
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM Semiconductor Corporation — DATE: 04/10/08

DESCRIPTION: 20-Pin, 209-Mil Wide, SSOP

PACKAGE CODE: H20

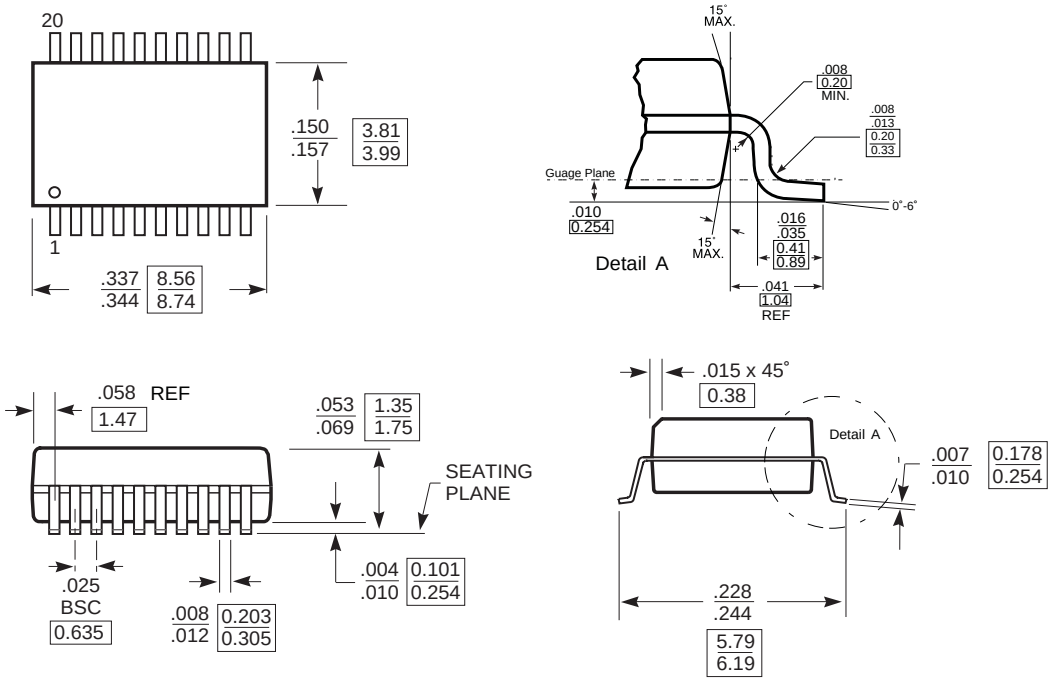
DOCUMENT CONTROL #: PD-1240 — REVISION: E

08-0140

Packaging Mechanical: 20-Pin 150-Mil QSOP (Q)

DOCUMENT CONTROL NO.
PD - 1202

REVISION: H
DATE: 10/22/07



X.XX
X.XX DENOTES DIMENSIONS IN MILLIMETERS

Note:
1) Controlling dimensions in inches.
2) Ref: JEDEC MO-137B/AD
3) Dimensions do not include mold flash, protrusions or gate burrs

Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 20-Pin, 150-Mil Wide, QSOP

PACKAGE CODE: Q

Ordering Information(1,2,3)

Ordering Code	Package Code	Speed Grade	Package Type
PI49FCT807TQE	Q	Blank	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT807BTQE	Q	B	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT807CTSE	S	C	Pb-free & Green, 20-pin 300-mil SOIC
PI49FCT807CTQE	Q	C	Pb-free & Green, 20-pin 150-mil QSOP
PI49FCT807CTHE	H	C	Pb-free & Green, 20-pin 209-mil SSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X Suffix = Tape/Reel